

**1.2.3.AK Binary Numbers and Conversion**

**Introduction**

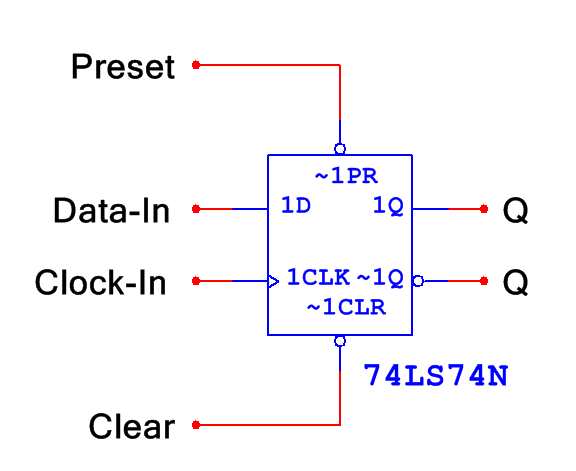
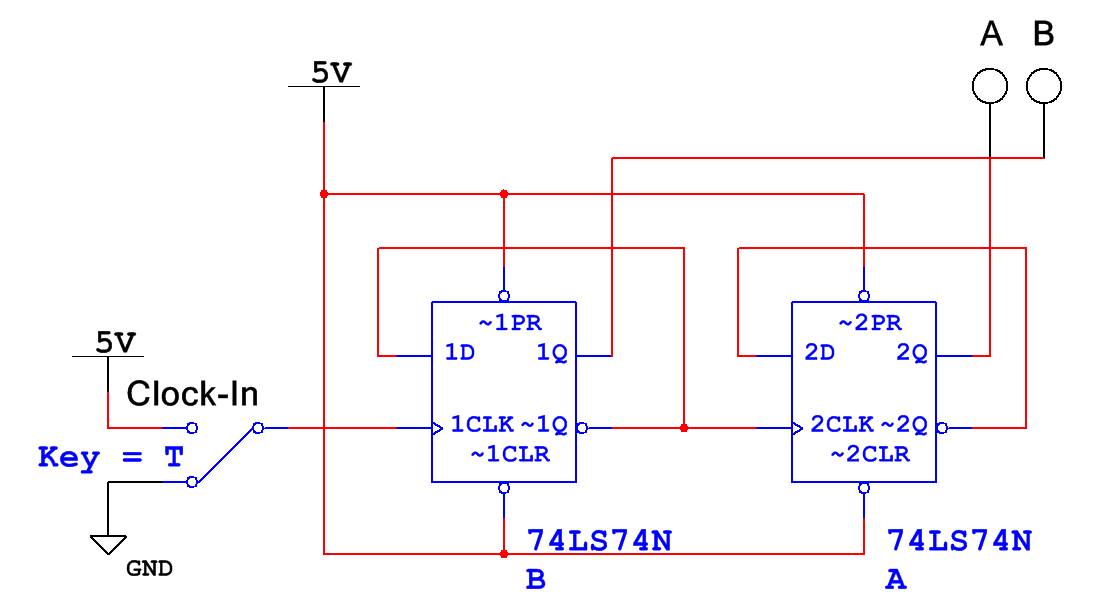
Along with combinational logic, sequential logic is a fundamental building block of digital electronics. The output values of sequential logic depend not only on the current input values (i.e., combinational logic), but also on previous output values. Thus, sequential logic requires a clock signal to control sequencing and memory and to retain previous outputs.

In this activity we will use the D flip-flop introduced in the previous lesson. We are limiting our use to this type of flip-flop in this introductory unit because of its simplicity and ease of use. The D flip-flop is just one of many different types of flip-flops that can be used to implement sequential logic circuits.

Equipment

* Circuit Design Software (CDS)
* (2) - 74LS74 Integrated Circuits (ICs)
* #22 Gauge solid wire
* Breadboard

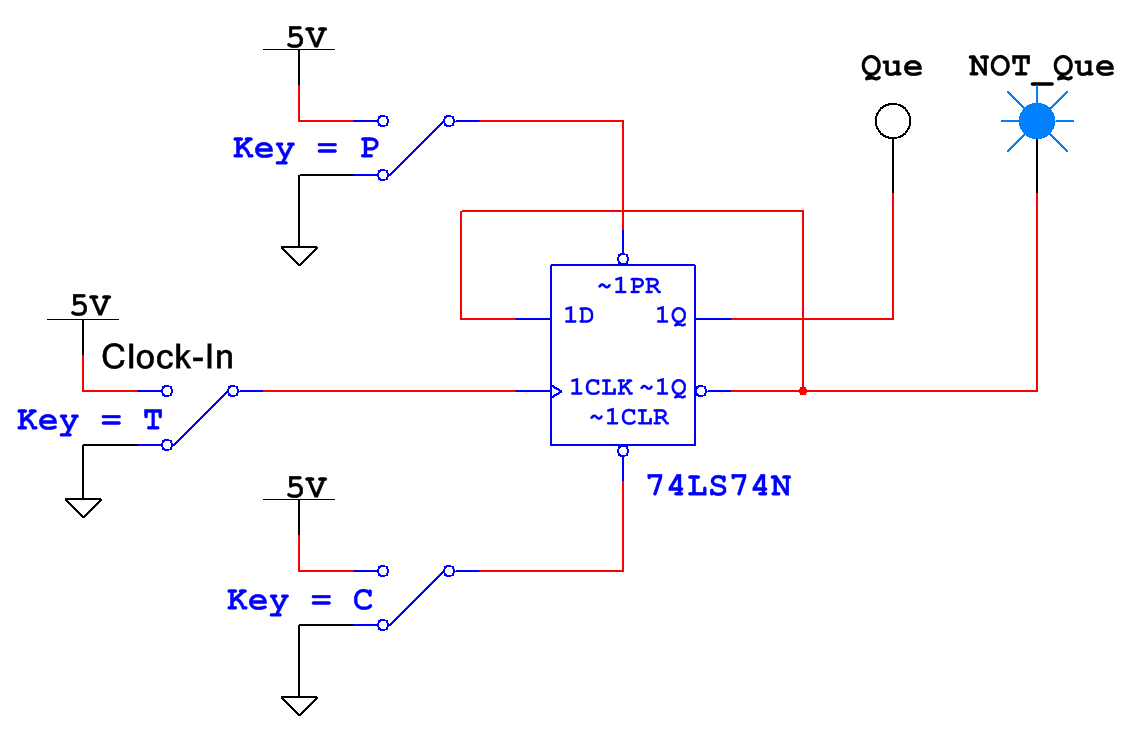
D Flip-Flop Example Circuit: Binary Counter



Procedure

Let’s begin the study of sequential logic by reviewing the basic operations of the D flip-flop.

1. Using the Circuit Design Software (CDS), create the circuit below.



* 1. Start the simulation.
  2. Set the input switches ***P*** and ***C*** to 5v. Again, since PR and CLR are active low inputs, this will make them both inactive. Toggle the input ***T*** several times. The circuit should behave exactly like the circuit in Activity 1.1.6.
  3. Set the input switch ***P*** to GROUND and ***C*** to 5v.

What is the state of the two outputs?

**Que is on. NOT Que is off.**

* 1. Toggle the input ***T*** several times.

Record what effect this has on the two outputs.

**No change. The flip-flop is “preset” to “1”.**

* 1. Set the input switch ***P*** to 5v and ***C*** to GROUND.

What is the state of the two outputs?

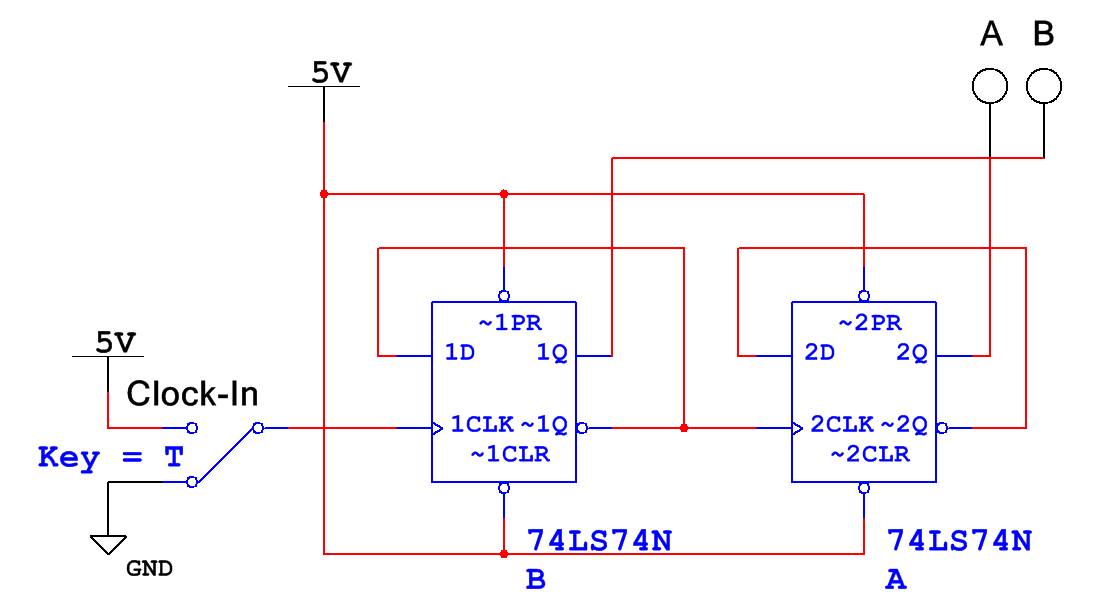
**Que is off. NOT Que is on.**

* 1. Toggle the input ***T*** several times.

Record what effect this has on the two outputs.

**No change. The flip-flop is “cleared” to “0”.**

1. Let us examine a simple binary counter. Counters are one of the most common applications of flip-flops. The circuit that we will be observing is called a two-bit binary counter. The counter will count from zero (00 in binary) to three (11 in binary).



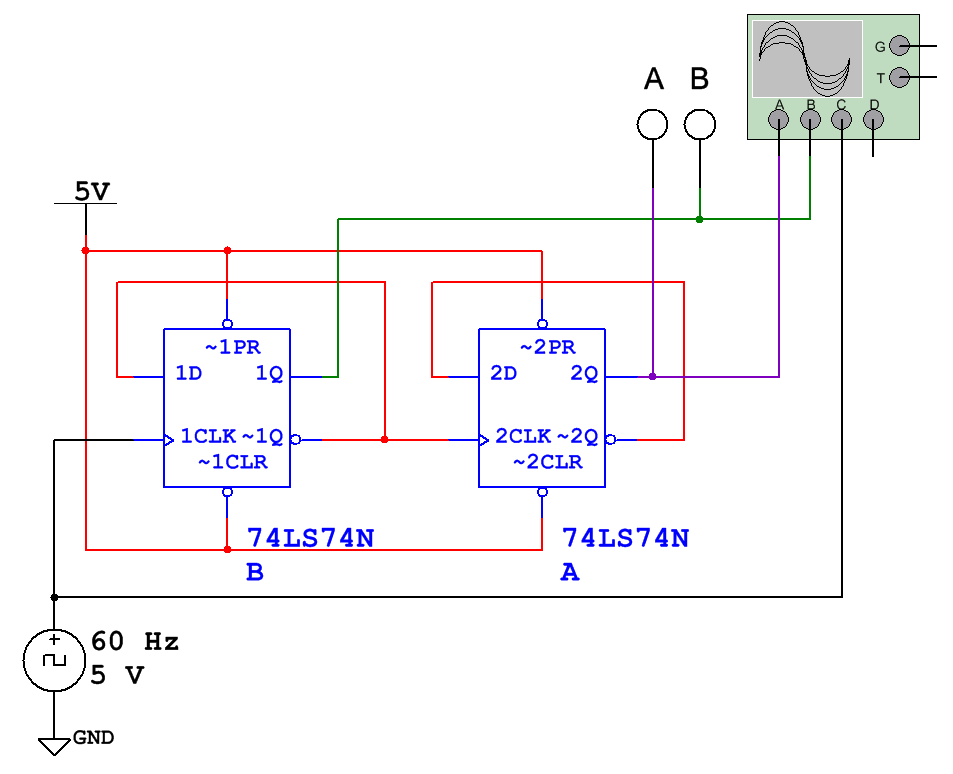
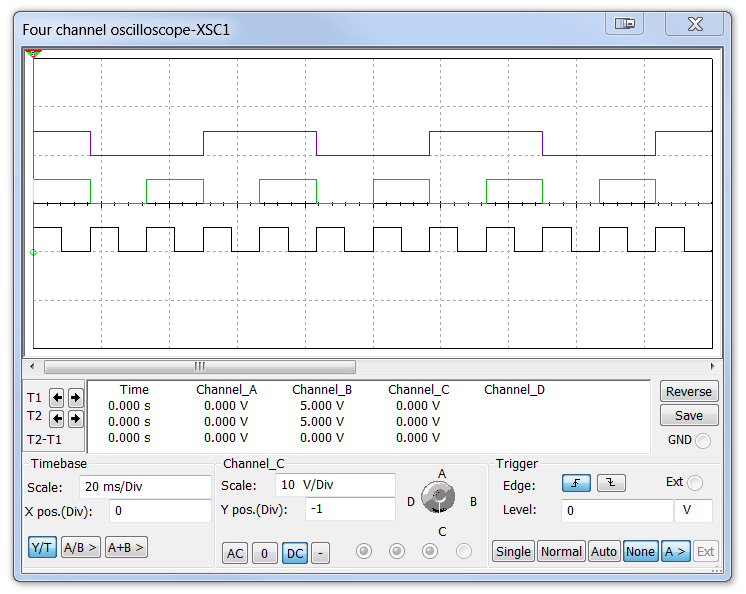
1. Using the Circuit Design Software (CDS), enter the two-bit binary counter shown below. Use a switch for the input ***Clock-In*** and probes for the outputs ***A*** and ***B***.
   1. Start the simulation.
   2. In Activity 1.1.6 we learned that the output on the first flip-flop (A) changes *only* when the Clock-In goes from low to high. Toggle the input ***Clock-In*** (switch ***T***)until **both outputs A and B are both low and switch *T* is low**. Now cycle switch ***T*** (*Cycle means to toggle from low to high back to low*) and record what effect this has on the two outputs in the table below.

|  |  |  |
| --- | --- | --- |
| **Clock-In** | **A** | **B** |
| **Initial Values** | **0** | **0** |
| 1st Cycle of switch ***T*** | **0** | **1** |
| 2nd Cycle of switch ***T*** | **1** | **0** |
| 3rd Cycle of switch ***T*** | **1** | **1** |
| 4th Cycle of switch ***T*** | **0** | **0** |
| 5th Cycle of switch ***T*** | **0** | **1** |
| 6th Cycle of switch ***T*** | **1** | **0** |
| 7th Cycle of switch ***T*** | **1** | **1** |
| 8th Cycle of switch ***T*** | **0** | **0** |
| 9th Cycle of switch ***T*** | **0** | **1** |

Based on these results, explain the pattern that you observe in the two outputs.

**The clock changes A and output from A changes B.   
The outputs create a binary count from 0 to 3 (002 to 112).**

1. Using the Circuit Design Software (CDS), modify the circuit used in step (1) so that it matches that shown below.
   1. The first modification is to replace the switch input with a **CLOCK\_VOLTAGE**. This change will result in the input being continuously toggled. This allows the change to happen without a person needing to toggle the switch. Be sure the CLOCK\_VOLTAGE is set to 5 volts, 50% duty cycle, 60 Hz.
   2. The second modification is to add a four-channel oscilloscope set up to view the three signals ***A***, ***B***, and ***Clock-In***.
   3. Be sure to set the oscilloscope’s time-base to 20ms/div and the vertical bases of the four channels to 10volts/div. Also, adjust the Y position of the three channels such that the four signals are all clearly visible.



A

B

CLK

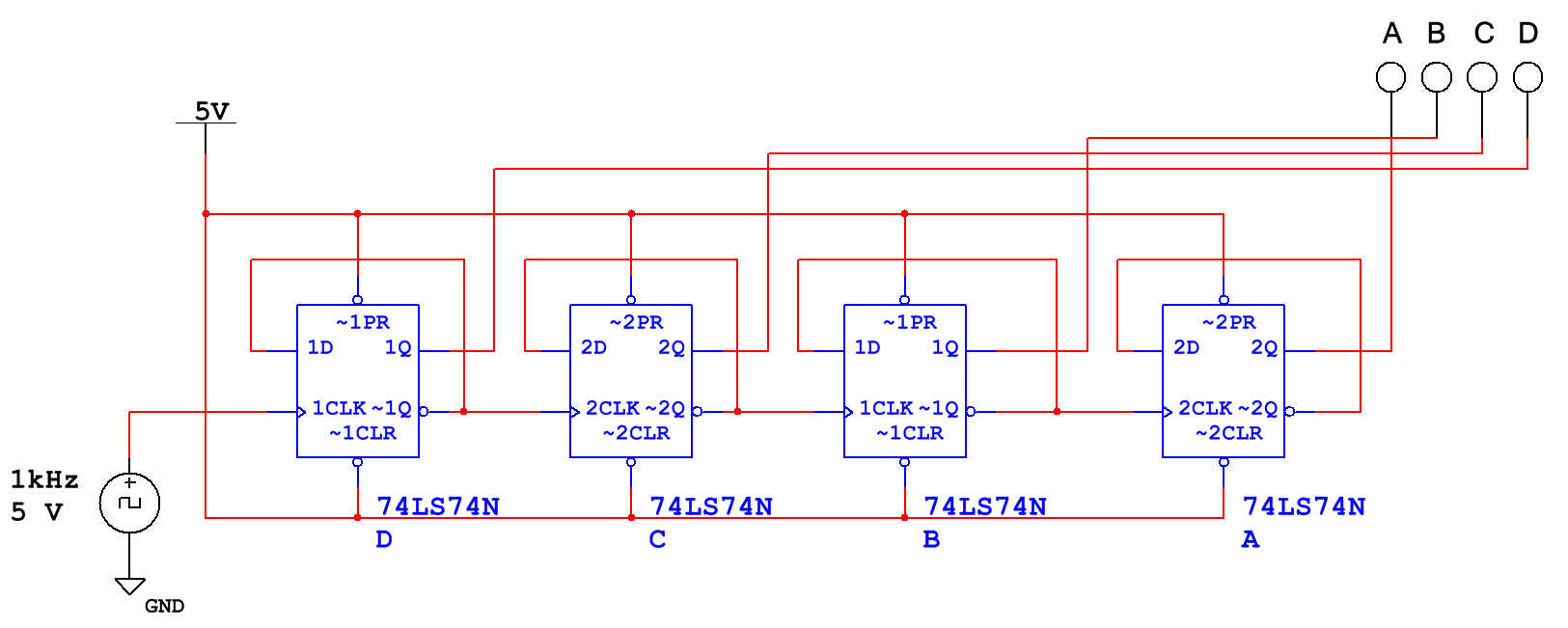
* 1. Start the simulation and let it run until you have captured several periods of each signal.
  2. Using the oscilloscope’s markers, measure the period of the three signals. Use this data to calculate the frequency for each signal. Record your data in the table below. Be sure to use the correct units.

|  |  |  |
| --- | --- | --- |
| **Signal** | **Period** | **Frequency** |
| **Clock-In** | **16.7 ms** | **60 HZ** |
| **B** | **33.4 ms** | **30 HZ** |
| **A** | **66.7 ms** | **15 HZ** |

* 1. Based on these results, explain the relationship of the period and frequency between the three signals. Was this expected?

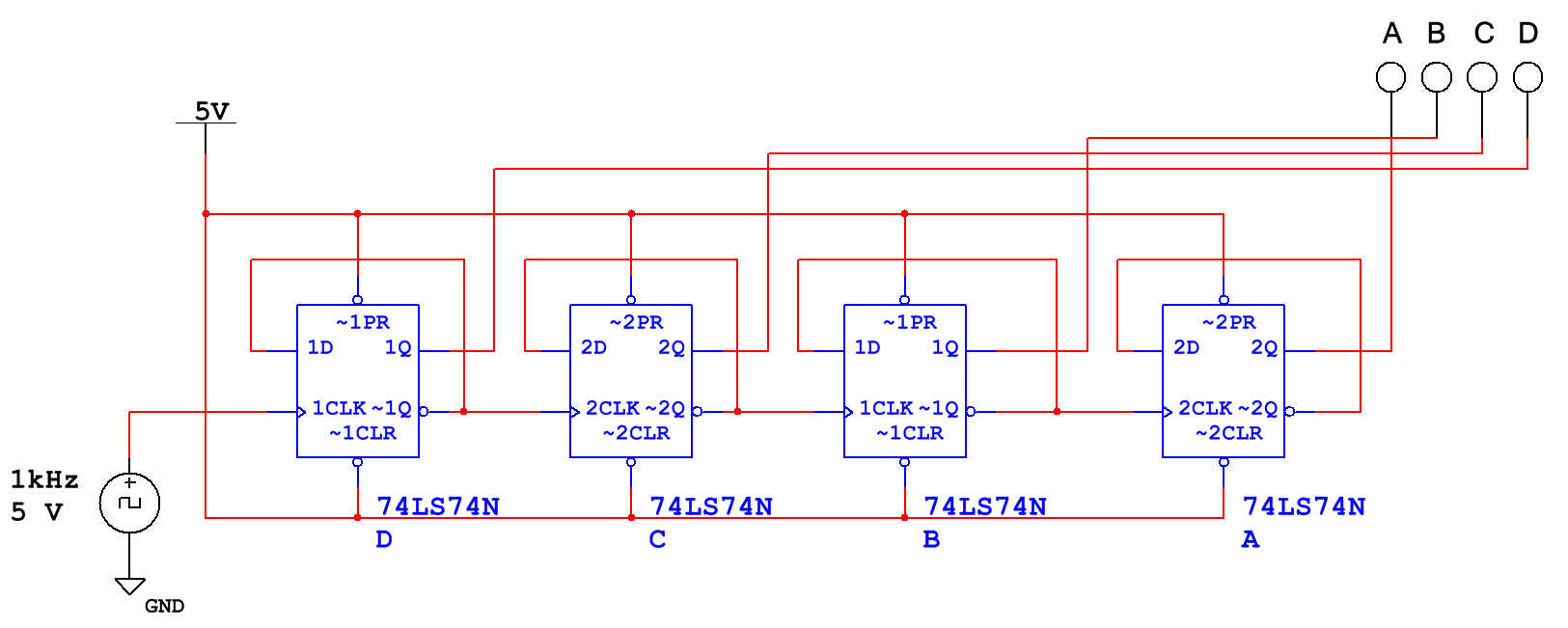
**Frequency and period are inversely related. The frequency gets cut in half each time a flip-flop is added to the design.**

1. Analyze the 4-bit binary counter shown below to determine the frequency and period for the signals A, B, C, and D. Use the table shown below to record your answers.

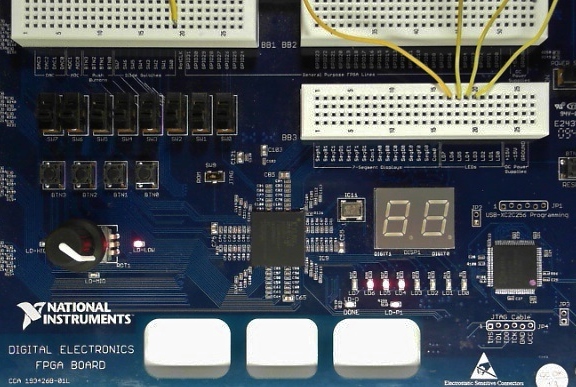


|  |  |  |
| --- | --- | --- |
| **Signal** | **Period** | **Frequency** |
| **Clock-In** | **1 ms** | **1000 Hz** |
| **D** | **2 ms** | **500 HZ** |
| **C** | **4 ms** | **250 HZ** |
| **B** | **8 ms** | **125 HZ** |
| **A** | **16 ms** | **62.5 HZ** |

1. With such a fast clock speed (1kHz) it is very difficult to see the binary count. Change the clock frequency to something that allows you to see the 4 probes transition more slowly in the simulation. Can you count to 15 in binary? What was the clock frequency that was best for you?
2. Using the pin diagram on the datasheet for the 74LS74 D flip-flop, create the 4-Bit counter you explored in this activity on your Digital Logic Board (DLB). Wire the four outputs to LD07, LD06, LD05, and LD04 of your Digital Logic Board (DLB). Wire the RotCLK to the CLK input of the first flip-flop.



rotCLK A B C D



1. Press the clock knob to select LD-Low. Turn the clock knob until you find a frequency you are comfortable with.
2. Have your instructor verify the counter is functioning.

**Conclusion**

1. The 2-Bit and 4-Bit counters you explored in this activity are referred to as “divide by two” counters. Explain the relationship between each consecutive flip flop and the order in which they are laid out in the design from right to left that creates a binary count.

**The frequency gets cut in half each time a flip-flop is added to the design.**

**If the outputs are arranged from lowest frequency to highest frequency from left to right, the outputs create a binary count.**

**With 4 flip-flops the count is 0 to 15 (00002 to 11112).**

1. If you added a 5th bit, what would you guess is the highest number you could count to?

**With 5 flip-flops the count is 0 to 31 (000002 to 111112).**

**16 + 8 + 4 + 2 + 1 = 31**

1. Can you think of 3-5 everyday items/products that might have a counter incorporated in them?

**Answers may vary.**

**Virtually all circuits in practical digital devices have a mixture of combinational and sequential logic.**

**Vending Machines**

**Security Alarms  
Thermostats**

**Electronic Battleship**

**Anything requiring memory**